CMOS ACTIVE PIXEL SENSOR (APS) OVER CCD FOR FUTURISTIC APPLICATIONS

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Abstract: *Sensors are becoming competitive with regard to Charged Couple Device (CCD) technology. They offer many advantages with respect to CCD, such as lower power consumption, lower voltage operation, on-chip functionality and lower cost. Nevertheless, they are still too noisy and less sensitive than CCDs. Noise and sensitivity are the key-factors to compete with industrial and scientific CCDs. It must be pointed out also that there are several kinds of CMOS Image sensors, each of them to satisfy the huge demand in different areas, such as Digital photography, industrial vision, medical and space applications, electrostatic sensing, automotive, instrumentation and 3D vision systems. In the wake of that, a lot of research has been carried out, focusing on problems to be solved such as sensitivity, noise, power consumption, voltage operation, speed imaging and dynamic range. In this paper, CMOS Image Sensors are reviewed, providing information on the latest advances achieved, their applications, the new challenges and their limitations.*

Keywords: *CMOS Image Sensors, Active Pixel Sensor (APS), Charged Couple Device (CCD)*

I. INTRODUCTION

In medicine and biotechnology, sensors are tools that detect specific biological, chemical, or physical processes and then transmit or report this data. Some sensors work outside the body while others are designed to be implanted within the body .Some monitoring devices consist of multiple sensors that measure a number of physical or biological parameters. Other devices may be multifunctional, incorporating sensors and then delivering a drug or intervention based on the sensor data obtained. Sensors may also be components in systems that process clinical samples, such as increasingly common "lab-on-a-chip" devices. Sensors help health care providers and patients monitor health conditions and ensure that they can make informed decisions about treatment. Sensors are also often used to monitor the safety of medicines, food, environmental conditions, and other substances we may encounter. Many different types of sensors are already used in health care, including self-care at home. Thermometers translate the expansion of a fluid or bending of a metal strip in response to heat into a number corresponding to body temperature. Paper-based home pregnancy tests contain a substance that changes colour in the presence of hormones indicating pregnancy. In hospitals and other provider-based settings, you can find more complex types of sensors like pulse oximeters (also known as blood-oxygen monitors), which measure changes in the body's absorption of special types of light to provide information on a patient's heart rate and the amount of oxygen in the blood.

Currently, there are many different Imaging Systems suitable for different purposes, de pending upon their final application. Digital Cameras, Camcorders, Webcams, Security cameras or IR-cameras are well-known Imaging Systems. Moreover, as the purposes are different, the technologies used differ from each other. This situation has been possible thanks to the fact that Imaging Technologies, mainly the ones concerning CMOS imagers, have been improving their performance, their functional capability and their flexibility during last year's.

CMOS image sensors have received much attention over the last decade, because their performance is very promising compared to CCDs. New horizons can be opened, like ultra low power or camera-on-chip systems. Owing to this situation and the latest developments within this field, this paper reviews CMOS image sensors.

In order to understand why CMOS image sensors have emerged as a strong alternative to CCDs, it is important, first, to highlight the Advantages and Disadvantages of CMOS image sensors.

II. ADVANTAGES AND DISADVANTAGES OF CMOS SENSORS

The main Advantages of CMOS imagers are:

1. Low power consumption. Estimates of CMOS power consumption range from one-third to more than 100 times less than that of CCDs. Besides, they work at low voltage. CMOS imagers only need one supply voltage, instead of CCDs, which need 3 or 4.
2. Lower cost compared to CCD's technology. On chip functionality and compatibility with standard CMOS technology. CMOS imagers allow monolithical integration of readout and signal processing electronics. A sensor can integrate various signal and image processing blocks such as amplifiers, ADCs, circuits for

colour processing and data compression, etc. on the same chip.
4. Miniaturisation, although important limitations exist, the level of integration is rather high.
5. Random access of image data.
6. Selective read-out mechanism
7. High-speed imaging. The flexibility and the possibility to acquire images in a very short period of time.
8. To avoid blooming and smearing effects, which are typical problems of CDD technology.

As outlined before, despite these advantages, there are still significant Disadvantages of CMOS image sensors compared to CCD technology. Therefore, these problems need to be solved so that CMOS image sensors can compete in any area. These disadvantages are:

1. **Sensitivity:** The basic quality criterion for pixel sensitivity is the product of its Fill Factor and its Quantum Efficiency where Fill Factor is the ratio of light-sensitive area to the pixel's total size, and Quantum efficiency is the ratio of photon-generated electrons that the pixel captures to the photons incident on the pixel area. It must be pointed out that Active Pixel Sensors (APS) have reduced sensitivity to incident light, due to a limited Fill Factor, hence, less quantum efficiency.
2. **Noise:** CMOS Image sensors suffer from different noise sources which set the fundamental limits of their performance, especially under low illumination.
3. **Dynamic range (DR):** Dynamic Range, which is the ratio of the saturation signal to the rms noise floor of the sensor, is limited by the photosensitive-area size, integration time and noise floor.
4. **Less image quality than CCD.**
   In order to overcome the disadvantages outlined before and, also, to improve the current advantages as well, the research on CMOS image sensors, has been mostly focused on the following areas:
   - Low noise
   - High dynamic range
   - High sensitivity and High fill factor
   - Low power consumption
   - Low voltage operation
   - High speed imaging

III. CMOS IMAGE SENSORS LIMITATIONS AND DEVICE SCALING CONSIDERATIONS

A. Industry trend

The technology has advanced from a 2 mm CMOS in 1993 to 0.25 mm in 1996 and less than 0.1 mm will also be possible. So, considering scaling effects has been necessary in order to know where and which are the limits of CMOS imagers.

Some Scaling Considerations were studied in 1996 and in 1997. The question was whether the image sensing performance of CMOS imagers would get better or worse as the technology would be scaled. The question arose because if CMOS imagers would scale down as fast as industry standard CMOS technologies, CMOS imagers would achieve a smaller pixel size than CCDs during the following years. Anyway, it seemed to be clear that 'standard' CMOS technology, which provided good imaging performance at 2–1 mm without any process change, would need some modifications in its fabrication process and innovations on the pixel architecture in order to enable CMOS imagers to perform good quality imaging when using the 0.25 mm generation technology and beyond. In fact, CMOS imagers could not be scaled down using standard CMOS technology because scaling effects increase leakage current and reduce dynamic range. That is to say that performance was getting worse. Thus, technological changes in CMOS technology are needed in order to reach the imaging performance of CCDs with a CMOS imager.

In 2000 a scaling perspectives study was done and, certainly, new technological processes appeared, such as PPD and TFA imagers.TFA imagers are immune to negative scaling impacts on sensitivity. Even more, they offer high sensitivity and high dynamic range. Nevertheless this technology is not suitable down to 0.1 mm. Thus, it has been demonstrated the limitation of conventional APS, because conventional pixel architecture (APS) cannot work properly with a 0.1 mm technology or below because the low power of these technologies implies a decrease in the saturation level and in the light sensitivity that it is not acceptable. Nevertheless, an alternative architecture called CAPS (Complementary APS) came on scene. They are a possible way to design a highly integrated, high performance CMOS image sensor in the deep sub-quarter micron technology, because CAPS architecture has a very attractive low-voltage operation capability.

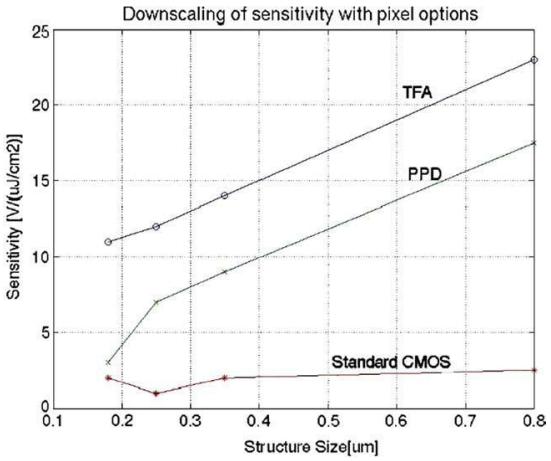

Fig.1. Downscaling of sensitivity with pixel options

IV. CMOS IMAGE SENSORS

CMOS image sensors are mixed-signal circuits containing pixels, analog signal processors, analog-to-digital converters, bias generators, timing generators, digital logic and memory.

A. Overall architecture

There are several CMOS imager topologies depending on their purpose. Nevertheless, CMOS

imagers architecture can be divided into four main blocks. Pixel Array, Analog Signal Processors, Row and Column Selector and Timing and Control.

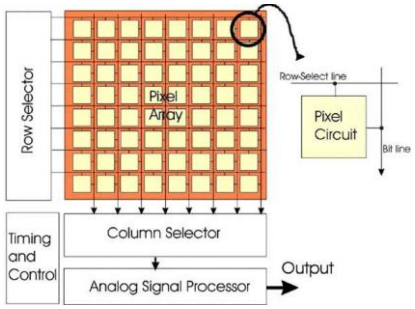

Fig.2. CMOS image sensor floor-plan.

B. Pixel circuits

Traditional imagers or photo-detectors

- **Photodiodes:** Semiconductor devices responsive to high energy particles and photons. They operate by absorption of photons or charged particles and the collected electrons which decrease the voltage across the photodiode in a proportional basis to the incident power. Currently, photodiode CMOS pixels are the most popular ones.
- **Photo-gates (PG) or CID (Charge-injection device):** Semiconductor devices that also collect the photon-generated electrons, but only when the photo-gate is biased to a high potential.
- **CCD (Charge-coupled device):** Device architecture based on series and parallel connection of capacitors, which are made using a dedicated semiconductor process.

Pixel circuits are mainly divided into active pixels (APS) and passive pixels (PPS). APS are sensors that implement a buffer per pixel. This buffer is as simple as adding a source-follower. Currently, APS are the predominant devices, although in some cases PPS are also used.

1) Passive pixels (PPS): They were the first CMOS imagers. They are based on photodiodes without internal amplification. In these devices each pixel consists of a photo detector (e.g. photodiode), and a transistor in order to connect it to a readout structure. Then, after addressing the pixel by opening the row-select transistor (RS), the pixel is reset along the bit line and RS. In spite of the small pixel size capability and a large fill factor, they suffer from low sensitivity and high noise due to the large column's capacitance with respect to the pixel's one.

2) Active pixels (APS): APS are sensors that implement a buffer per pixel. This buffer is a simple source-follower. It is well known that the insertion of a buffer/amplifier into the pixel improves the performance of the pixel. Power dissipation is minimal and, generally, less than CCD's, because each amplifier is only activated during readout. Nevertheless, it must be noted APS technology has some disadvantages: Conventional APS suffer from a high level of fixed pattern noise (FPN) due to wafer process variations that cause differences in the transistor thresholds and gain characteristics. A solution is to use a Correlated Double Sampling (CDS) circuit, which can almost eliminate the threshold variations that cause offsets in the video background.

3) Photodiode (PD) type APS: The photodiode-type (PD) APS is considered as standard and it was described by Noble in 1968. It consists of three-transistor: a reset transistor, for resetting the photodiode voltage and a source follower with select transistor, for buffering the photodiode voltage onto a vertical-column bus. The PD APS is suitable for most mid low-performance applications.

4) Photo-gate (PG) type APS: It was introduced later than PD APS, in 1993 and it employs the principle of operation of CCDs concerning integration transport and readout inside each pixel. Its transfer of charge and correlated double sampling permits a low noise operation. Thus, it is suitable for high performance and low light applications.

5) Logarithmic APS: Non-linear output of the sensor can be desirable. This fact permits an increase on the intra-scene dynamic range. Logarithmic APS are suitable for High Dynamic Range applications, although they suffer from large FPN. Owing to this fact, currently, they are not as used as before. It must be pointed out that they are used a lot in silicon retinas.

6) CTIA APS pixels: As highlighted before, conventional APS suffer a high level of FPN. Thus, reducing FPN has been a challenge for quite a while and some solutions have been reported.

For instance, capacitive trans-impedance amplifier (CTIA) pixels can achieve low FPN. Besides this, the high gain and low read noise are advantages of using CTIAs as well. Fig. 3h and g show a high FPN and low FPN CTIA APS pixel schematics respectively.

7) Pinned photodiode (PPD) pixel: The pinned photodiode, which was previously used in charge-coupled devices, was proposed early during the development of CMOS active-pixel image sensors. Besides lower pixel noise, the pinned photodiode offers reduced dark current. Therefore, they are a PG's alternative, because their architecture offers higher sensitivities than PG.

8) TFA pixels: The thin film on ASIC (TFA) pixels were developed in order to improve sensitivity. They consist of an amorphous silicon (a-Si:H) multilayer system that is deposited on top of an ASIC. Their absorption coefficient for visible light is approximately 20 times bigger than crystalline's silicon (c-Si). In fact, TFA pixels are suitable for High Dynamic Range applications.

9) Complementary active pixels sensors CAPS: CAPS are a possible way to manufacture a highly integrated, high performance CMOS image sensor in the deep sub-quarter micron technology. Furthermore, CAPS architecture has low power consumption and a high low-voltage operation capability. The main new features are that the reset transistor is replaced by a PMOS. In addition, a complementary signal path is implemented and the

pixel gives out two signal path outputs: V_{outn} and V_{outp}.

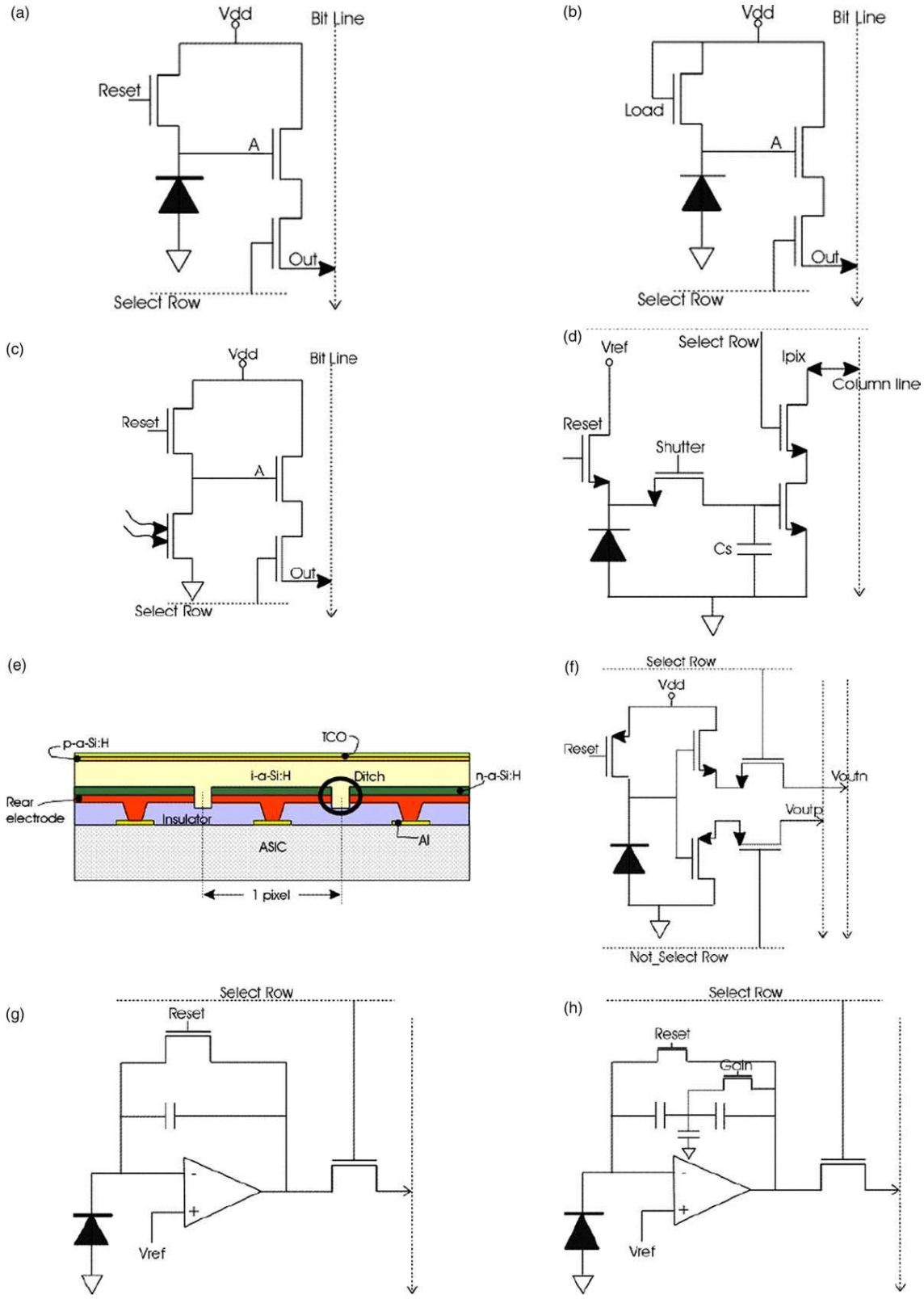

Fig. 3.(a) A photodiode- type APS schematic, (b) A photodiode- type logarithmic APS schematic, (c) A photo-gate- type APS schematic, (d) Photodiode- type shutter APS schematic, (e) TFA pixel, (f) A photodiode- type CAPS schematic, (g) A photodiode- type Low FPN CTIA APS schematic (h) A photodiode- type High FPN CTIA APS schematic.

10) Other pixels. There is more pixel architectures, due to the huge number of possible applications. For instance, pixel circuits suitable for high speed operation by adding a shutter transistor.

Overall, PG, PPD and TFA are detector structures to improve the sensitivity. Nevertheless, TFA provides significantly better values than PPD due to the higher fill factor and higher quantum efficiency.

C. Analog Signal Processing

Analog signal processing circuits are used in order to improve the performance and functionality of CMOS image sensors. However, they tend to involve less pixel density and increase the chip area due to the added functions. Some research has been done to overcome these problems.

Firstly, there are some well known traditional signal processing systems. For instance, additional analog-signal-processing circuitry located at the periphery of the array permits the suppression of both, temporal and fixed-pattern noise. As an example, Correlated Double Sampling (CDS) or Double Differencing Sampling (DDS) suppress FPN. Others achieve high SNR and ADC for camera-on-a-chip. Secondly, there are also several signal processing systems depending on the application. For instance, signal processing such as K-winners-take-all, are suitable for 3D vision systems and sub-pixel accuracy. Smoothing, motion detection, programmable amplification, multi-resolution imaging, video compression, dynamic range enhancement, discrete cosine transform (DCT), intensity sorting, etc. are other signal processing systems.

1) Readout methods

Readout methods have an important influence in the sensor performance. Thus, there are several readout methods depending on the desirable application. The main requirements are:

1. low power dissipation
2. high resolution
3. good linearity
4. stable detector bias
5. low noise
6. high injection efficiency
7. small pixel size
8. good dynamic range

APS readout structures fulfil 4 and 8 requirements, but not 3 and 7. On the other hand PPS readout structure fulfils 7 and not 3, 4, 6 and 8. Finally, share-buffered direct-injection (SBDI) readout structure combines both imagers characteristics.

Therefore, it is possible to find suitable traditional readout methods for low FPN, for high frame rates, to increase linearity and DR, with high SNR and ultrahigh- sensitivity and for infrared detectors. Finally, there are also specialised readout methods suitable for ultra high sensitivity, for focal plane array, for X-ray imaging, for an emission-transmission medical imaging systems, for low-light levels, detectors with self-triggered readout, offset-free column readout circuit and transversal-readout architecture

2) Noise sources

CMOS Image sensors suffer from several noise sources. They set the fundamental limits on image sensor performance, especially under low illumination and in video applications. Therefore it is important to have an overview of all of them.

The noise sources in CMOS imagers can be divided into Temporal Noise and Fixed Pattern Noise (FPN).

3) Temporal noise

It can be divided into different kinds of noise, depending on its source:

- Pixel noise: photon shot noise, reset or kT/C noise (which is the thermal noise resulting from resetting after each pixel's readout. The k is Boltzmann's constant, T is the absolute temperature; and C is the junction parasitic capacitance), dark current shot noise and MOS device noise (thermal, 1/f or flicker, etc.)
- Column Amplifier noise
- Programmable gain amplifier noise
- ADC noise
- Overall temporal noise, noise floor or reading noise.

4) Fixed pattern noise (FPN)

It has been a huge CMOS imagers' limitation. FPN is the fixed variation in the output between pixels when a uniform input is applied. In a perfect image sensor, each pixel should have the same output provided that the same input is applied, but in current image sensors the output of each sensor is different. FPN does not change as a function of time and can be characterized, assuming a linear pixel response, as a variation in the offset and gain at each pixel.

VI. LATEST DEVELOPMENTS IN THE FIELD OF CMOS IMAGERS

The research has been mainly focused on APS in areas like Low noise, High dynamic range, High sensitivity and High fill factor, Low power consumption, Low voltage operation, High speed imaging. To remark is that all these features are difficult to achieve in one design. Hence, depending on the application, one feature will have more priority than another one.

A. High dynamic range (DR)

The ratio of the saturation signal to the rms noise floor of the sensor is known as dynamic range. This is limited by the photosensitive-area size, integration time and noise floor, which is the noise generated in the pixel and the signal processing electronics. DR is limited by the integration time, although high dynamic range image readout can be achieved by using different exposure or integration times.

Secondly, with respect to the noise floor the use of a linear readout is more suitable than a logarithmic one. So Dynamic Range of CMOS APS is strongly managed by the readout method. Finally, the photosensitive-area size is an important issue because of the well-known scaling effects.

The major problem of artificial image acquisition has been the extraordinary high optical dynamic range of natural scenes. For instance, the

human vision system exhibits an enormous optical dynamic range of about 200 dB, due to the fact that it can adapt to an extremely high range of light intensity levels. Nevertheless, artificial imagers have been much poorer in this aspect. With conventional CCD sensors it is hard to reach high dynamic range and CMOS imagers with logarithmic response suffer from excessive FPN and temperature drift. For instance, in year 2000 the conventional CCD imagers exhibited usually a DR of about 50–70 dB only and on the other hand, CMOS imagers would achieve better DR, up to 140 dB, than CCDs, although they used logarithmic readout, which has some disadvantages such as a high FPN.

In fact, some research has been done to obtain CMOS image sensors with high dynamic range:

1) Logarithmic

The use CMOS imagers with logarithmic readout or the non-linear output of the logarithmic pixel provides higher dynamic range. Nevertheless, logarithmic response has a large FPN and slower response time for low light levels, which bring down the image quality. Thus, some systems based on logarithmic response have been developed in order to offer high DR with low FPN. For instance, in 1998, the University of Heidelberg proposed a CMOS camera chip with logarithmic response and self-calibrating FPN correction. Its results showed a significant FPN reduction. Fraunhofer Institute of Micro-electronic Circuits and Systems of Duisburg suggested also a CMOS imager with Local Brightness adaptation. It used logarithmic image sensors in order to reach high DR and FPN was also compensated. In year 2000, S. Kavadias reported a technique to remove the high FPN, due to its logarithmic response. This CMOS image sensor, which was based on an active pixel structure, employed on-chip calibration and achieved a DR of 120 dB and the FPN was 2,5% of the output signal range. Finally in year 2003 a multi-resolution scheme and a cost-effective architecture for nonlinear analog-to-digital conversion was presented. These two features combined together improve the sensors quality under low light intensity.

2) Linear

On the other hand, using CMOS imagers with linear readout can improve FPN, even though they can achieve lower DR than logarithmic ones. The response was linear, low FPN was achieved and DR was of 69 dB. In year 2000 a CMOS image sensor for automotive applications was proposed. It offered a high dynamic range up to 120 dB and an excellent image quality due to its linear readout. Furthermore, it had good temperature behaviour up to 85 *8*C. In year 2002 a high dynamic CMOS imager with spiking pixels, pixel-level ADC, and linear characteristics was reported. It had a DR of 93 dB, although 120 dB was expected. Finally, it is reported of a mechanism, using linear readout, capable for adjusting its sensitivity depending on the absolute illumination level, like human vision. This is reached by using different integration times. The results demonstrate that with 1 integration time, a DR of 61 dB is reached. In contrast, with two integration times, the DR is of 92 dB.

3) Combined

In 1998, the University of Waterloo reported a CMOS APS with combined linear and logarithmic mode operation. The results showed that it had good linearity, in the linear mode operation, and it reached wide dynamic range in the logarithmic mode.

So the issue is to determine which is the more convenient readout method in each application. Nevertheless, using linear readout methods with different integration times seems to be more suitable.

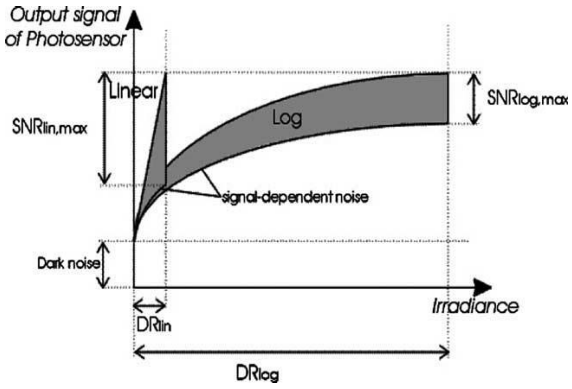

Fig.4. Photo conversion characteristics: linear vs logarithmic

4) TFA technology

As outlined before, TFA technology is suitable for achieving a high dynamic range and a high fill factor. In 1999–2000, T. Lule reported a 100.000 pixel imager in TFA technology. The main feature was that every pixel contained an automatic shutter, which adapted the integration time to the local intensity. This allowed obtaining a high DR of 120 dB.

B. High sensitivity (High fill-factor (FF) and high quantum efficiency)

The basic quality criterion for pixel sensitivity is the product of its Fill Factor and its Quantum Efficiency, Where Fill Factor is the ratio of light-sensitive area to the pixel's total size; also known as aperture efficiency, and Quantum efficiency is the ratio of photon-generated electrons that the pixel captures to the photons incident on the pixel area. Photons are lost for conversion due to: reflection on dielectrics, no absorption in the acquisition layer and loss of charges and recombination.

It is well known that a good image quality is obtained if most of the chip area is dedicated to the photo-detectors. Therefore in order to achieve a good image quality, a high Fill Factor (FF) is needed. Unlike CCDs, which achieve around 100% FF, CMOS APS FF are limited, because each pixel has an area devoted to the CMOS readout circuitry.

Around 30% FF is a kind of standard. In CMOS APS pixel, the Fill Factor is limited by: (a) shadowing by metals or silicides, (b) collection of photons by the insensitive junctions of the active pixel, (c) the relatively small size of the useful photo-sensitive junction, (d) recombination of photo-generated carriers with majority carriers, limiting the diffusion length. Besides this, a high fill factor allows shorter exposure times for a given pixel size or smaller pixel sizes for a given sensitive area. Thus, FF plays an important role in the scaling perspectives and imager's performance.

In the wake of that, a lot of research has been done to increase the fill factor of CMOS APS. There are different methods used to improve the FF: one is to design active pixels with larger photodiodes, although small pixels cannot be made and large photodiodes have low charge conversion sensitivity due to their higher capacitance. The other method is to make passive pixels, but their performance with respect to active pixels is worse. On the other hand, micro-lenses, which help funnelling photons to the light-sensitive portion of the pixel, are another alternative to overcome this problem. They could reach up to 90% Fill Factor. In spite of this 90% Fill Factor, they have some disadvantages such as the reduction of efficiency as micro-lens dimension decreases. In fact, some high fill-factor designs based on CMOS APS exist, which can enhance the FF: A. Bermak developed a 46% Fill Factor native logarithmic pixel in 0.7 mm CMOS technology in 2000. In 2002, the Georgia Institute of Technology achieved a fill factor greater than 40% by using a matrix transform imager Also in 2002, National Tsing-Hua University described an APS, with a fill factor of 55%, made in 0.25 mm technology. In addition, this device has a high DR of 120 dB, thanks to its innovative tuneable injection current compensation architecture and a voltage operation of 1.9 V.

Finally, it is important to consider the downscaling effects, because small pixels mean lower light sensivity and dynamic range. Thus, conventional APS technology is limited. Nevertheless innovative architectures, ideas and technologies reaching a fill factor up to 90–100% have appeared.

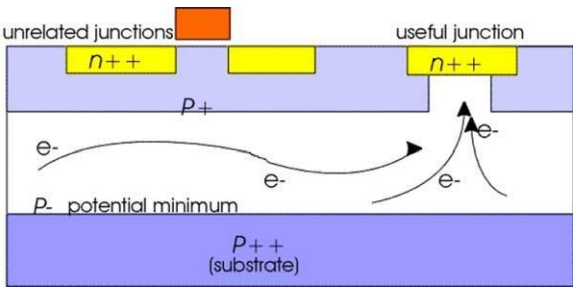

Fig. 5. Cross-section of Fill Factory's well pixel.

Photoelectrons are channelled by electrostatic barriers shielding them off the active pixel circuitry and substrate, to the photodiode junction. Virtually, all electrons diffuse down this drain, and as the diffusion time is short (typically 10–50 ns) negative effects like image lag must not be feared.

In addition, TFA Imagers offer 100% FF. The photodiode is placed on top of the ASIC. So the whole pixel area is available for the photodiode and there are no further layers obstructing the light penetration such as further metallization, polysilicon or dielectrics.

Increasing the photosensitivity of the photo-detector is another thing to be taken into account in order to improve the quantum efficiency. M.Furumiya reported in 2001 a high photosensitivity and no-crosstalk pixel technology for an APS by using a 0.35 mm CMOS technology. A deep p-well photodiode, with a sensitivity improvement of 110% for 550 nm incident light, and an antireflective film to increase photosensitivity, consisting of Si_3N_4 film, with a sensitivity improvement of 24% are used. Finally, it is possible to increase the sensitivity by the cascoding method, which allows shielding of the integrating capacitor from the parasitic junction capacitance of the photodiode. This can be done with shutter APS or CTIA pixel.

C. High performance (low power consumption and low voltage operation)

One of the most important advantages of CMOS image sensors compared to CCDs is the lower power consumption. Therefore, CMOS image sensors are suitable for portable applications, among which, cellular phones, portable digital assistants (PDAs), and wireless security systems, etc.

A lot of research has been carried out on this topic. Low power camera-on-a-chip using CMOS APS technology began to be developed in 1995 by NASA at the Jet Propulsion Laboratory and in 1998, the first CMOS APS fabricated using a high performance 1.8 V, 0.25 mm technology was introduced by Hon-Sum Philip Wong. In that paper, the impact of the device scaling was studied, because no process modifications were made to the CMOS logic technology. In 1999, a CMOS imager with a power consumption of 250 mW with an acquisition rate of 60 frames/s and a resolution of 1280:720 pixels was reported. This has been useful for large-format high-speed imaging applications such as industrial vision systems. In 2000, a 1.2 V micro-power CMOS Active Pixel Image Sensor for portable applications was proposed. In 2001, a low voltage hybrid Bulk/SOI CMOS APS was manufactured. Also, in 2001, Nara Institute of Science and Technology reported a CMOS pixel circuit based on a pulse frequency modulation (PFM) technique. This device reached a quite good performance (DR over 50 dB) under very low operation voltage, less than 1 V, and was very robust against noise due to its A/D converter. In 2003, a 176:144 CMOS APS with micro-power consumption was reported, with a voltage operation of 1.5 V and power consumption of 550 mW. Thus, this amount enables the sensor to run using a watch battery.

Other novel designs have been introduced, like a CMOS imager with motion vector estimator for low power image compression, which was designed by Toyohashi University of Technology in 1999.

Someone states that APS will not function at 1.2 V or below. However, CAPS offer to work with a low voltage of 1 V or less using advanced technologies. They claim to obtain good performances. Unlike APS, it must be stressed that CAPS are an alternative architecture which can be manufactured using top level technologies, below 0.25 mm, with great performance (see device scaling considerations). Thus, Low Voltage systems expect to continue downscaling by using CAPS, as an alternative to conventional APS.

D. High speed imaging

Acquiring high-speed images is becoming more and more important in some areas such as real time applications. Nevertheless CCD technology did not make enough progress in this aspect. During more than 3 decades CCDs have been developed and after spending millions of dollars, they reached 250 kilo-pixels with an acquisition speed of 1000 frames per second. Comparatively, high speed CMOS sensor technology is just started, because the first high-speed sensors were introduced around 1998 and they have reached already great results. In addition, high frame rates have been possible thanks to the CMOS downscaling. In conclusion, CMOS imagers appear to be a promising alternative to CCDs taken also into account other advantages such as less Blooming and Smearing effects.

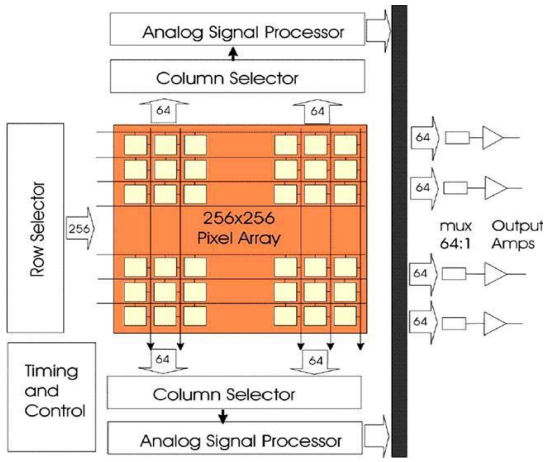

Fig.6. Architecture of the high speed CMOS imager.

1) Needs and problem solving

A typical CMOS APS contains three NMOS transistors in each pixel only. Therefore, a very compact implementation is possible although the sensor lacks of image data parallel acquisition, a feature often important in high-speed imaging. The alternative is a pixel that contains an analog memory called SNAP (Shuttered-Node Active Pixel). Another important issue is how the data is multiplexed into the output pads. Multiplexing of digital data is much simpler than passing off analog data, so ADC are needed. Another architectural feature that allows high-speed operation is pipelining.

A CMOS image sensor needs to full fill all the necessary requirements in order to provide fast image acquision. No smear, no blooming and global electronic shutter are some of the most valuable characteristics needed. In addition, low lag and snap-shot mode are preferable. Low lag is essential in order to capture rapidly changing scenes. The rolling shutter method is very common in CMOS imagers where the rows of pixels in the image sensor are sequentially reset, starting at the top of the image and proceeding row by row till the bottom. When this reset process has moved some distance down the image, the readout process begins: rows of pixels are read out sequentially as well, starting at the top of the image and proceeding row by row till the bottom in exactly the same fashion and at the same speed as the reset process. So, this device is not appropriate at high frame rates, because the scene can significantly change during the frame reading time. Therefore, a non-rolling shutter or snap-shot mode is necessary. It is also necessary to acquire images in a very short time and using short integration times. This requires the image sensors to be equipped with synchronous shutter in order to avoid blur. For instance, images acquisition of fast-moving objects requires imagers with high photo-responsivity at short integration times, synchronous exposure, and high-speed parallel readout.

2) High speed market

High speed imaging systems are suitable for automotive applications such as occupancy detection, pre-crash sensing, collision avoidance, surveillance, crash test observation, or airbag control. For instance, a smart airbag solution based on a high speed camera system was designed by Fraunhofer Institute of Microelectronic Circuits and Systems. The system continuously monitors the seats and quickly determines the occupancy status and passenger's position and size before the airbag is blasted. Another application is smart image sensor for real-time. For instance Yosuke Oike reported in 2003 a smart image sensor for real-time and high-resolution 3D measurement. It does not only have enough high frame rate for real-time 3D measurement, but also high pixel resolution owing to a small pixel circuit and high sub-pixel accuracy due to gravity centre calculation using a light intensity profile measurement trick. Finally, an application for high-speed video systems, for fast moving objects or for machinery vision is also suitable.

E. Low noise sensors

CMOS Image sensors suffer from several noise sources. These set the fundamental limits on image sensor performance, especially under low

illumination and in video applications. Therefore, it is important to have an overview of all of them. The noise sources in CMOS Imagers can be divided in Temporal Noise and Fixed Pattern Noise (FPN).

In fact, FPN is one of the major CMOS imager's disadvantages. Thus, a lot of research has been done in order to minimise FPN.

Many researchers have designed FPN-reduction circuits. For instance, Correlated Double Sampling (CDS) is one of the most suitable for suppressing FPN.CDS technique consists of taking two samples from a signal, which are closely spaced in time. Then, the first signal is subtracted from the second one, hence, removing the low-frequency noise. Sampling occurs twice: first after reset and last after integrating the signal charge. The subtraction removes the reset noise and dc offset from the signal charge. The two values are then used as differential signals in further stages like programmable gain amplifiers (PGA) or ADC. However, CDS reduces the fixed pattern noise to a large extent, a component of the FPN due to mismatch in the CDS circuits at each column introduces column-FPN, which should be also removed. For instance, K. Yonemoto and H. Sumi proposed that FPN reduction should be performed in a CDS circuit, in order to avoid this column-FPN caused by CDS circuits. On the other hand, although the dark current variation of photodiodes appears as FPN in the output signal of a CMOS image sensor, which resembles FPN caused by threshold variation of transistors in pixel circuits, the dark current noise cannot be suppressed with CDS circuits. This is because the dark current does not appear in the reset level, but only in the signal level of the pixel signal. Therefore, the dark current of the photodiode itself should be reduced.

One way of reducing the dark current is to employ a pinned photodiode. Another method reported by K. Yonemoto and H. Sumi in 2000 is a pinned photodiode, in the form of hole accumulation diode (HAD). They achieved a reduction of the dark current to 150 pA/cm^2 instead of 6 nA/cm^2 of a pn-photodiode. As a result, the dark current variation at the output of the CMOS image sensor was 0.19 mV and the period of readout operation was about 20 ns at 30 frames/s. Two years later, K. Yonemoto and H. Sumi carried out a numerical analysis of this CMOS Image sensor with a simple FPN reduction technology. They showed that the low-input-voltage I–V converter with a current-mirror circuit improves the amplification factor and linearity of the pixel circuit. In a five-transistor pixel circuit, the threshold voltage of the X–Y addressing transistor affects the amplitude and the level of the readout pulse. An analysis of the mechanism of the X–Y addressing transistor showed the basic concept behind the selection of the threshold voltage. An L-shaped readout gate for a pinned photodiode was compared with a straight readout gate, and was proved to be adequate for rapid charge transfer.

Moreover, other readout methods can also offer an improvement in order to suppress FPN. For instance, R&D Headquarters from Minolta Co. and Gazoh System Kaihatsu reported a CMOS APS with transversal readout architecture that eliminates the vertically striped FPN. The possibility of high frame rate using a multiport structure was also demonstrated. In addition, the Photonics and Sensors Group of the Cambridge University suggested, in 2002, a new readout circuit for a CMOS APS, which removes the FPN and reduces signal degradation while offering an increase in readout speed compared to the conventional approach.

As outlined before, CDS cannot suppress the dark current noise, although it is a FPN's source Thus, decreasing the dark current to suppress FPN has been an aim. Dark current (offset error) is the signal charge that the pixel collects in the absence of light divided by the integration time. Dark current is temperature-sensitive and typically normalised by area. Photo bit Technology Corporation and Tokyo institute of Technology reported a low dark current stacked CMOS APS for charged particle detection.

A use of a p-MOSFET transistor for readout reduces the hot carrier effect; thereby the dark current within the low temperature region is greatly decreased. It also improves noise reading performance due to its lower flicker noise compared to n-MOSFETs'.

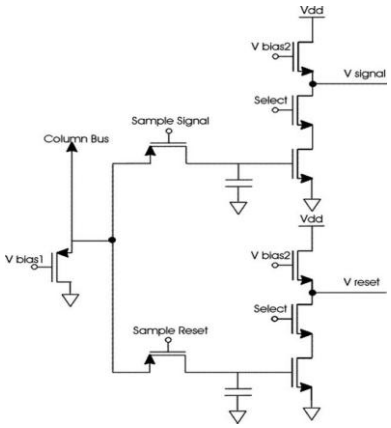

Fig.7 Schematic diagram of the correlated double sampling circuit. There is one such circuit for every column

. Thanks to the improvement of the noise performance, CMOS Image Sensors for Low light level applications are possible. In 2000, a CDS noise analysis of readout circuits used in CMOS APS for low light levels was carried out. In 2001, different pixel architectures were studied in order to increase the sensitivity and reduce the spatial (FPN) and temporal noise. This study demonstrates that the N-well photodiode is the best light sensor, either for its parasitic capacitance value, for its quantum efficiency, or for its dark current. However, the design rules required by this photodiode (a wide space must be kept between N well and MOS transistors) limit their use in CMOS imagers. On the other hand, a new pixel

architecture was also introduced. This architecture reduces kTC or reset noise and FPN. Therefore, this architecture is ideal for applications requiring very high sensitivity and low noise, which is necessary for low light level sensing.

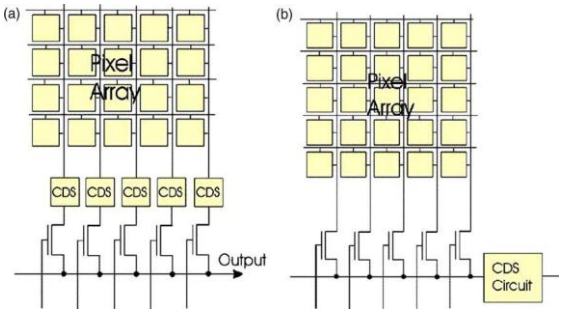

Fig.8. (a) CMOS image sensor with column CDS circuit, (b) CMOS image sensor with proposed FPN-reduction scheme

Complete reset of the photodiode is needed in order to remove kTC or reset noise and decrease the lag effect. Note that the source of image lag in CMOS imagers is different from the source of image lag in CCDs. In CCDs, image lag is caused by incomplete charge transfer. This can be eliminated using a pinned photodiode. On the other hand, CMOS image lag is due to incomplete reset so, in 2001, H. Tian reported a new reset method, which alleviates the lag without increasing the reset noise. The reset transistor gate is overdriven.

Finally, CMOS APS still has readout-noise problems because of irregular gain from mismatched transistor thresholds.

VII. APPLICATIONS

As highlighted before, improvement of CMOS image sensors has opened up new application areas Therefore, CMOS imagers are very suitable for Space, Auto-motive, Medical, Digital photography and 3D applications. Furthermore, there are more specific applications such as portable devices, security, industrial vision, consumer electronics, imaging phones, astronomy, surveillance, robotics and machine vision, guidance and navigation, computer inputs, etc.

VIII. CONCLUSION

A review of the most important advances in the field of CMOS image sensors has been carried out. These advantages have been mainly focused on fields such as sensitivity, low noise, low power consumption, low voltage operation, high-speed imaging and good dynamic range. This paper demonstrates that CMOS imagers are competitive with CCDs in many application areas, such as security, consumer digital cameras, automotive, computer video, imaging phones, etc. CMOS imagers will replace CCD devices in some cases, because of its low cost, low power consumption, integration capability, etc. Nevertheless, CCD technology will continue as predominant in high performance systems, such as medical imaging, astronomy, low-end professional cameras, etc.

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